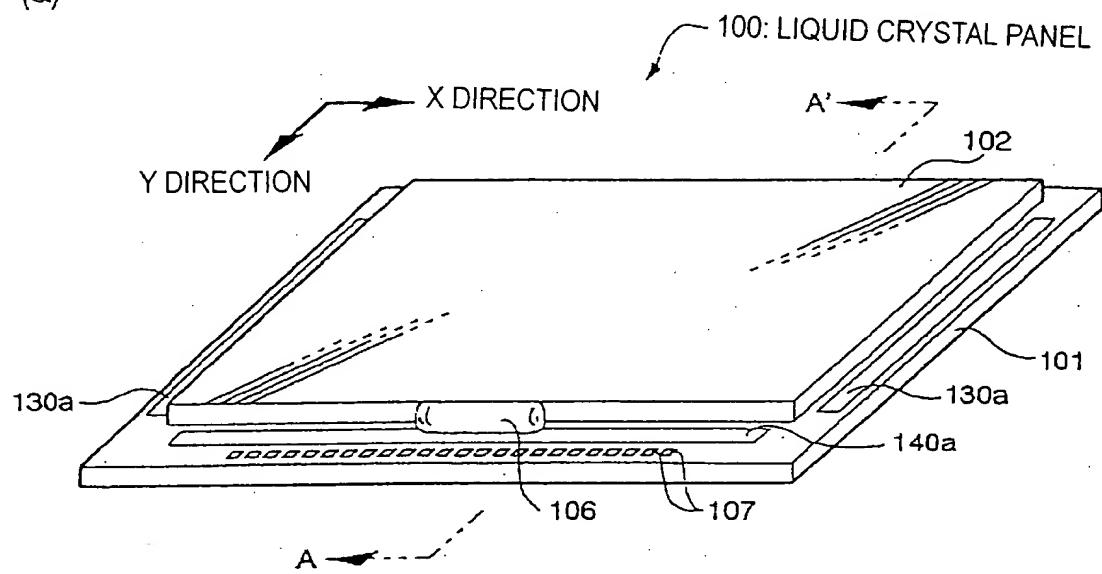


FIG. 1

(a)



(b)

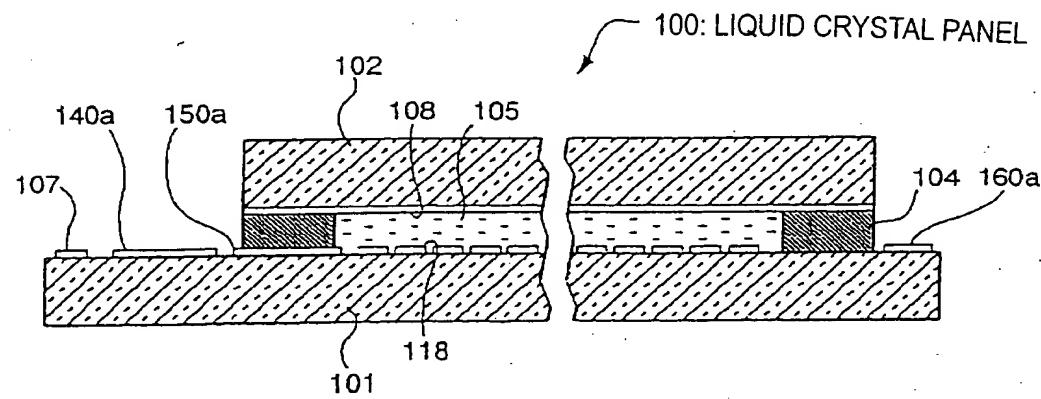


FIG. 2
101 102 103 104 105 106 107 108 109 110 111 112 113 114 115 116 117 118 119 120 121 122 123 124 125 126 127 128 129 130

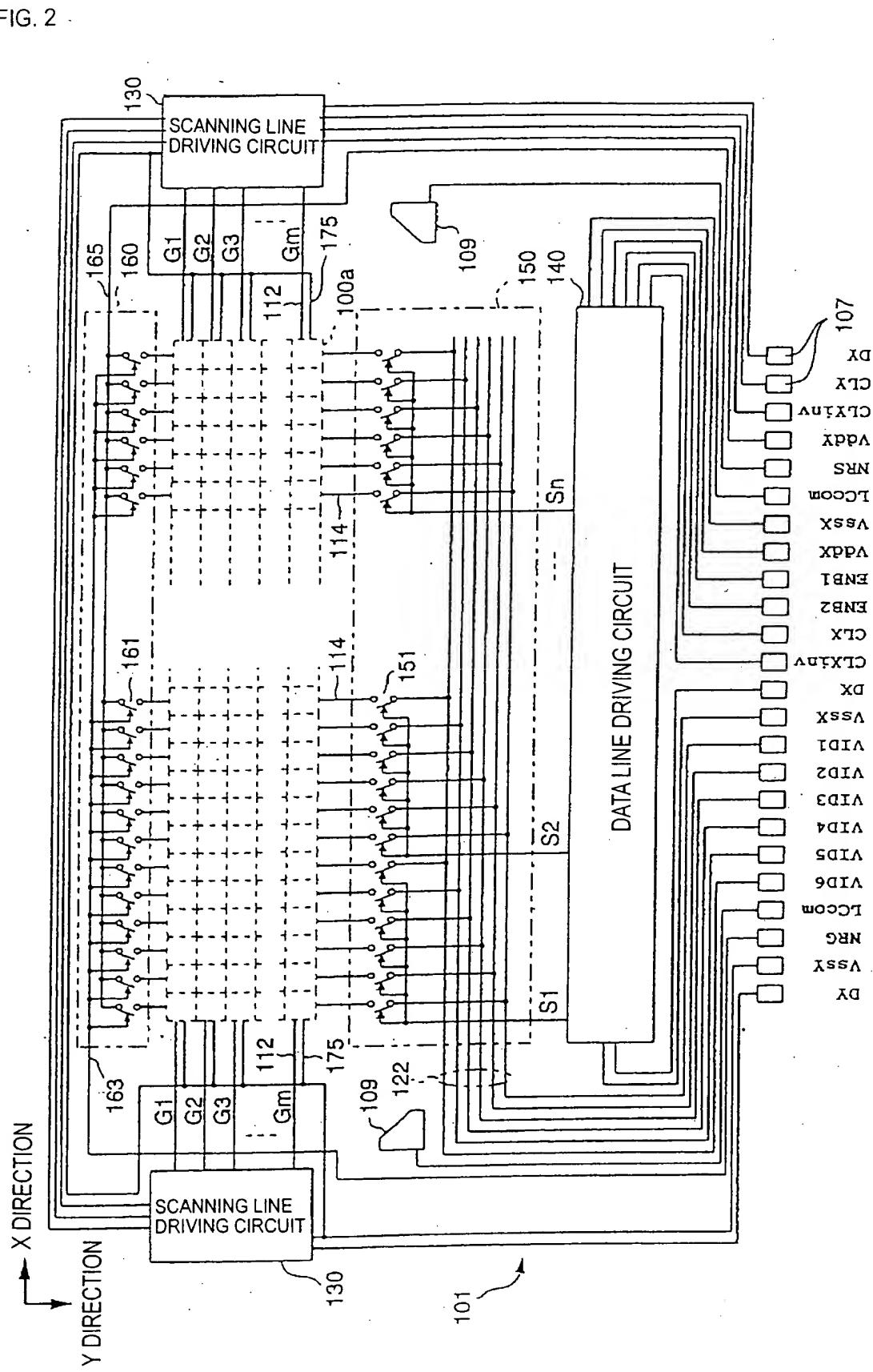


FIG. 3

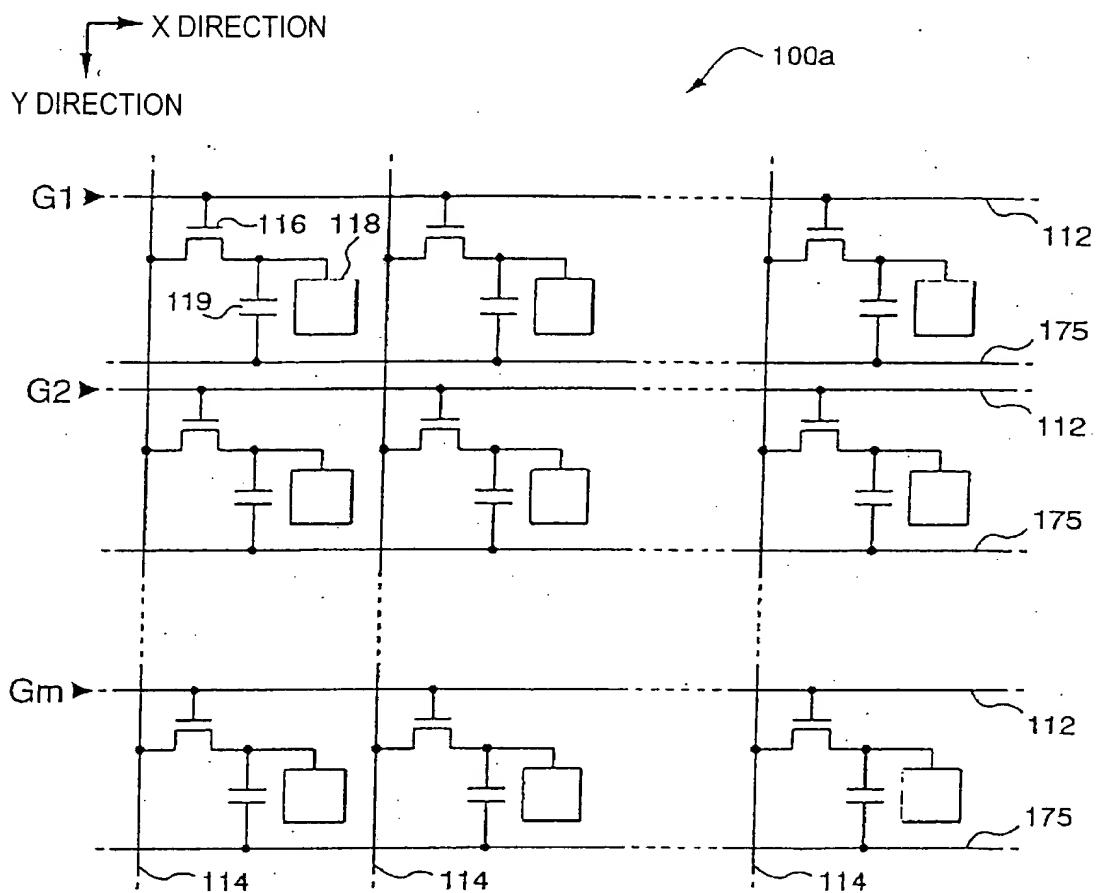


FIG. 4

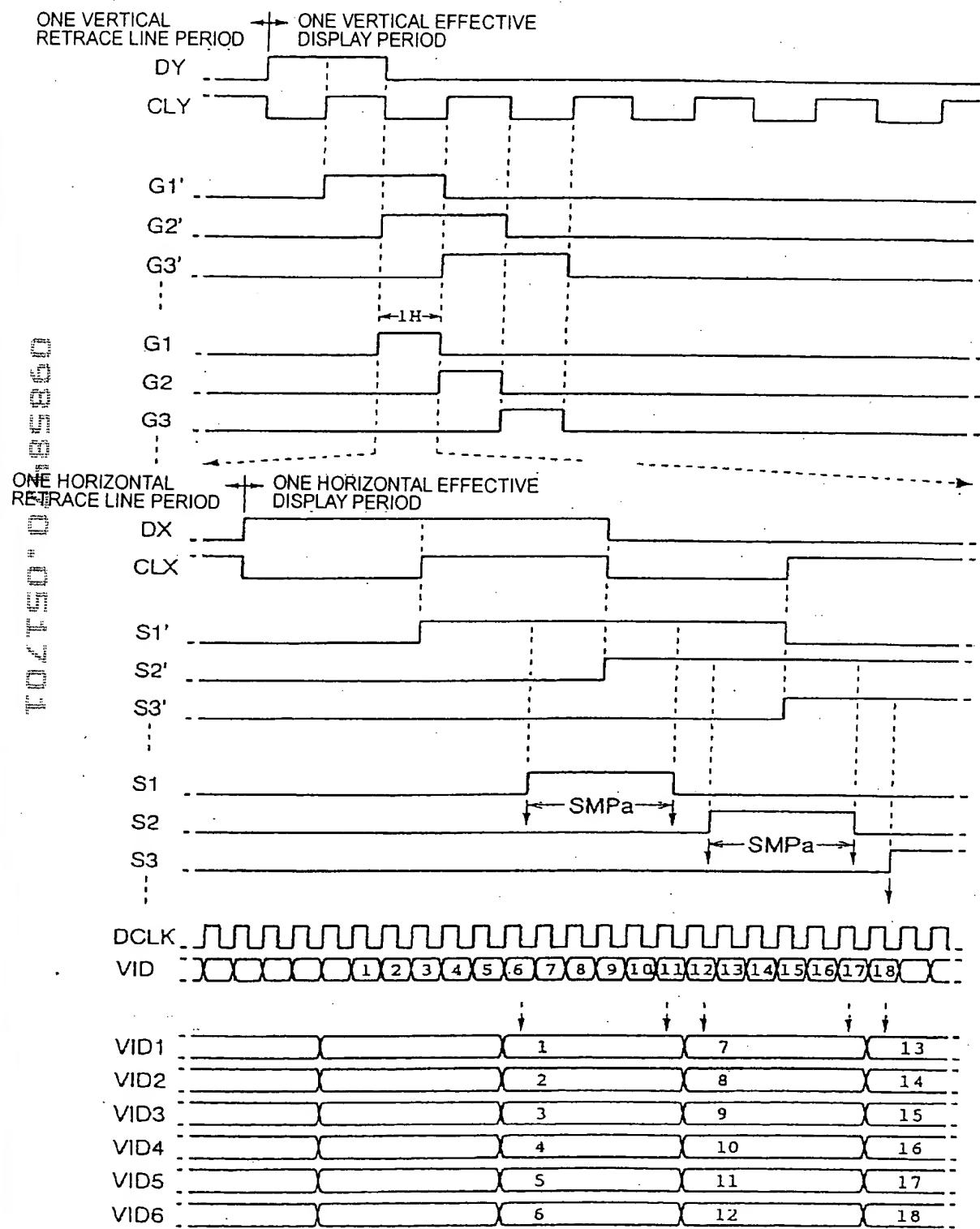


FIG. 5

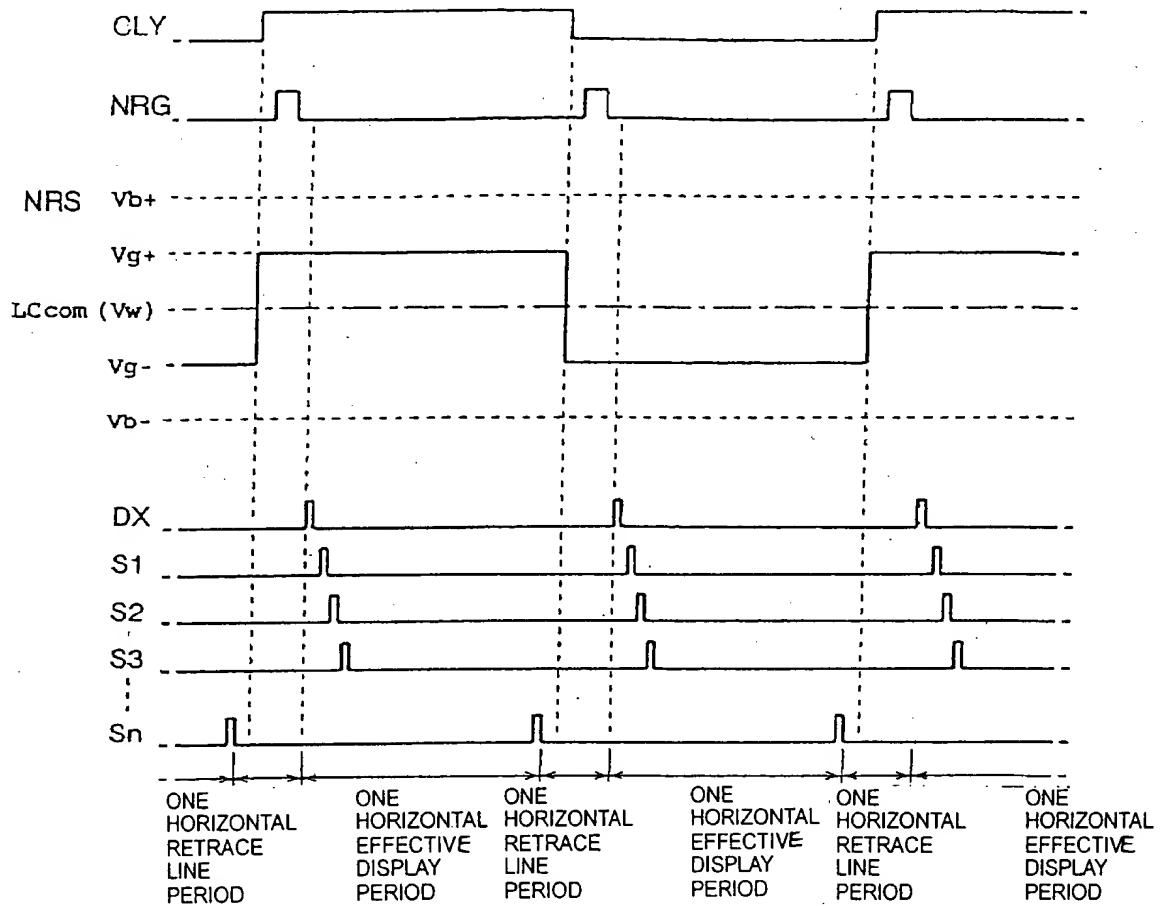


FIG. 6

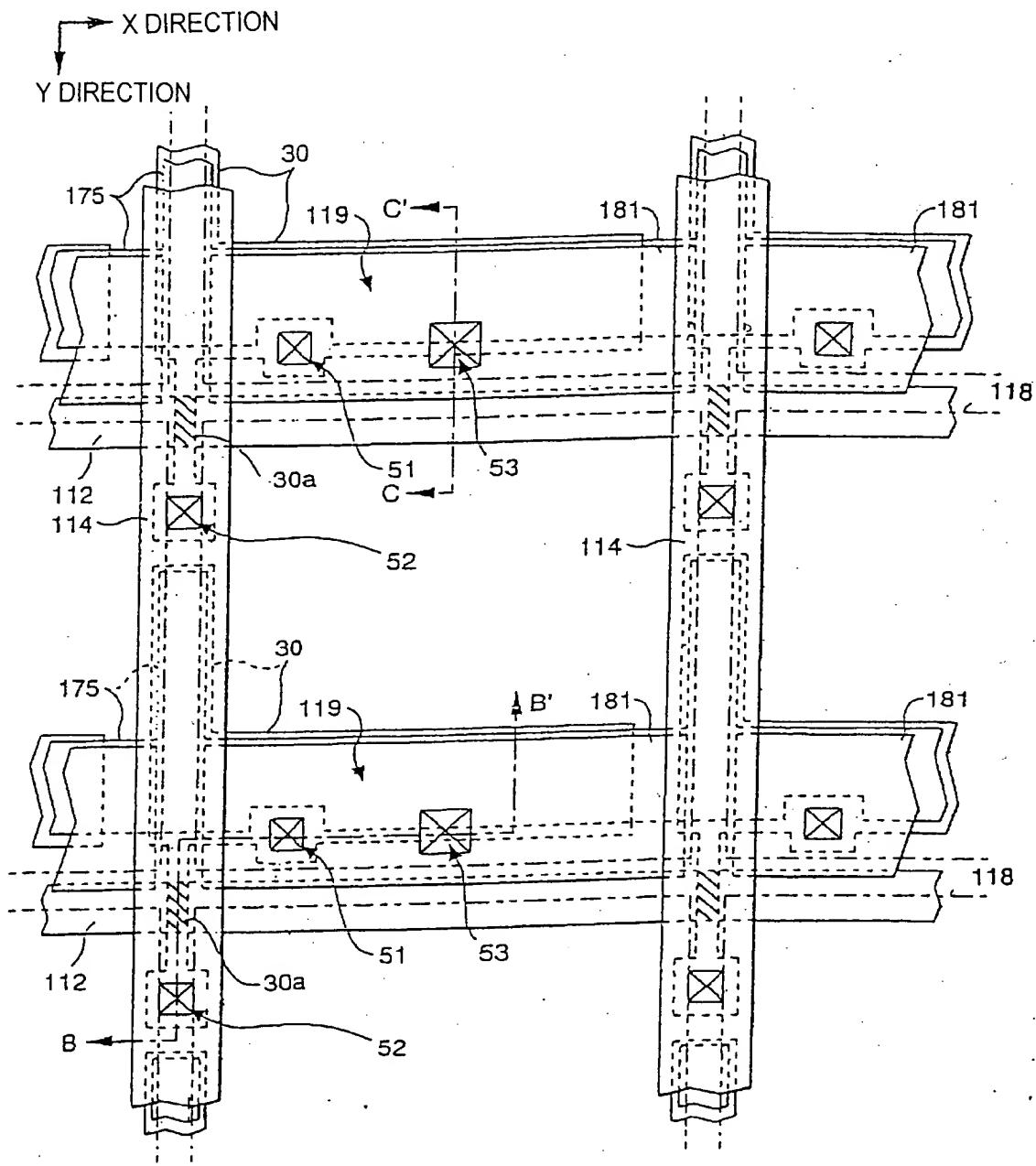
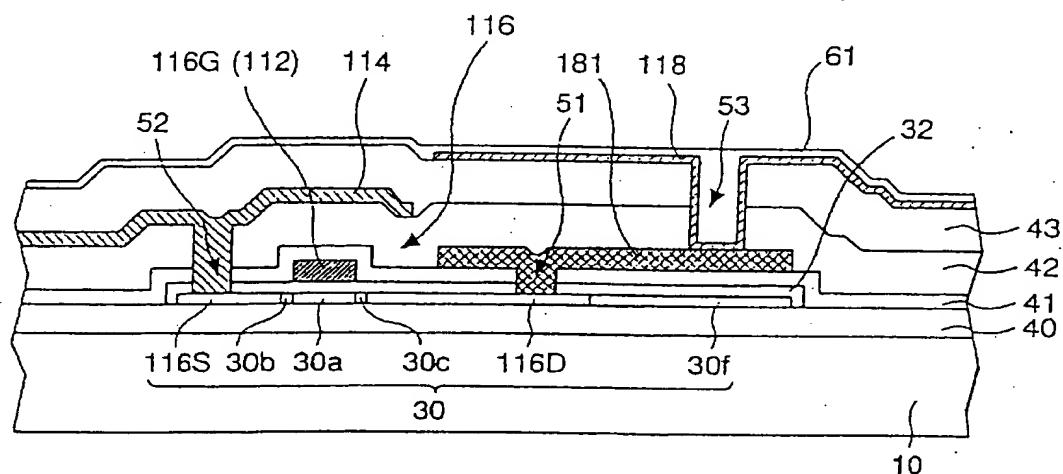
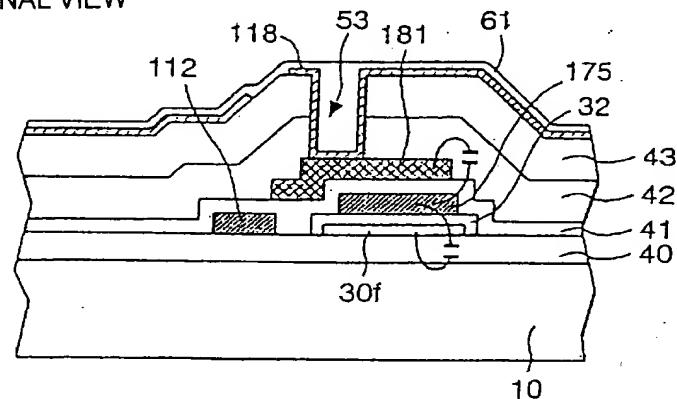


FIG. 7

(a) LINE B-B' CROSS-SECTIONAL VIEW



(b) LINE C-C' CROSS-SECTIONAL VIEW



(c) EQUIVALENT CIRCUIT OF STORAGE CAPACITOR

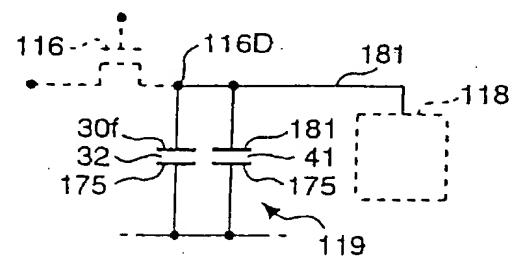


FIG. 8

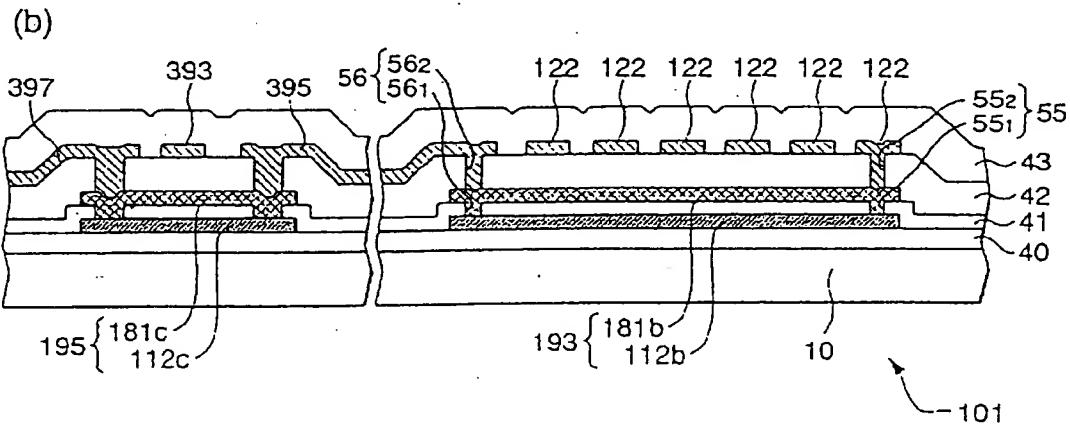
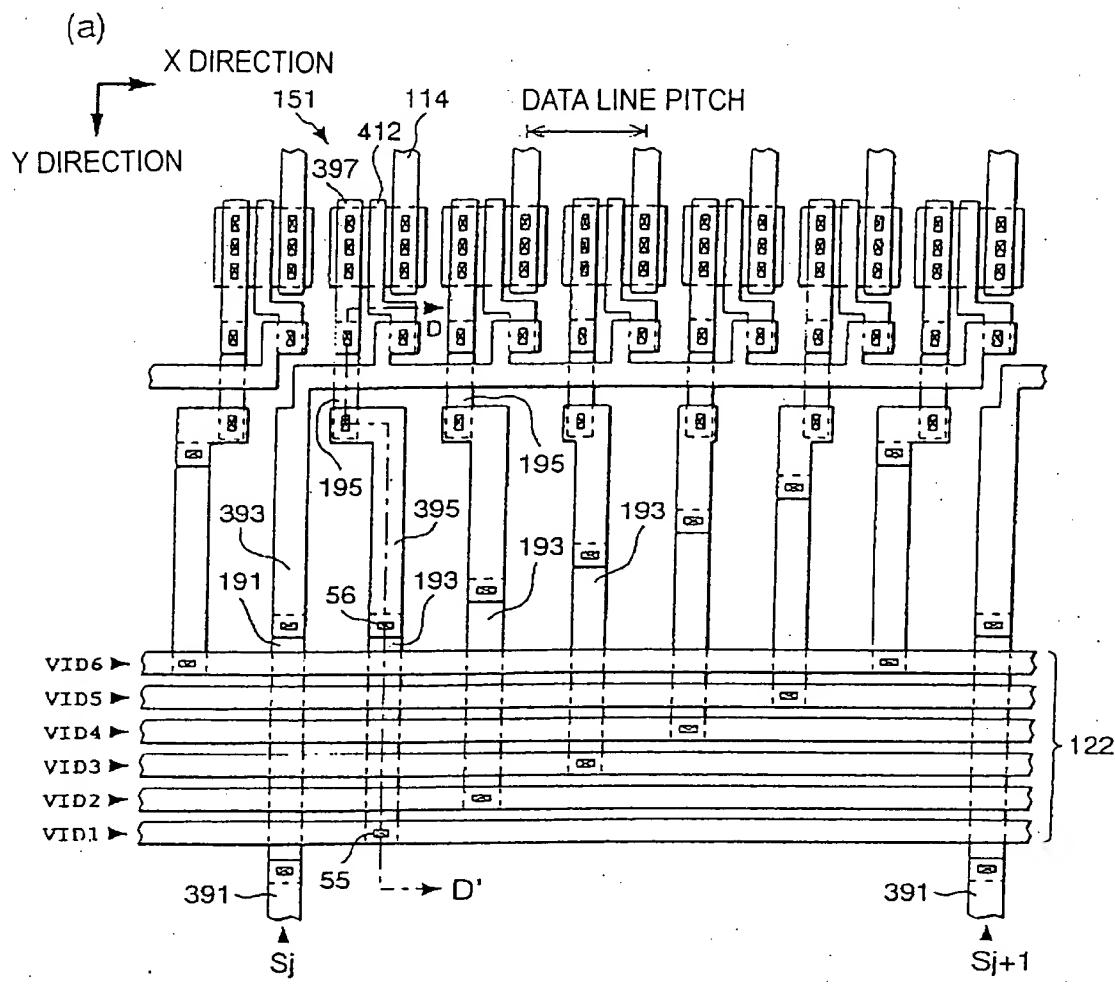
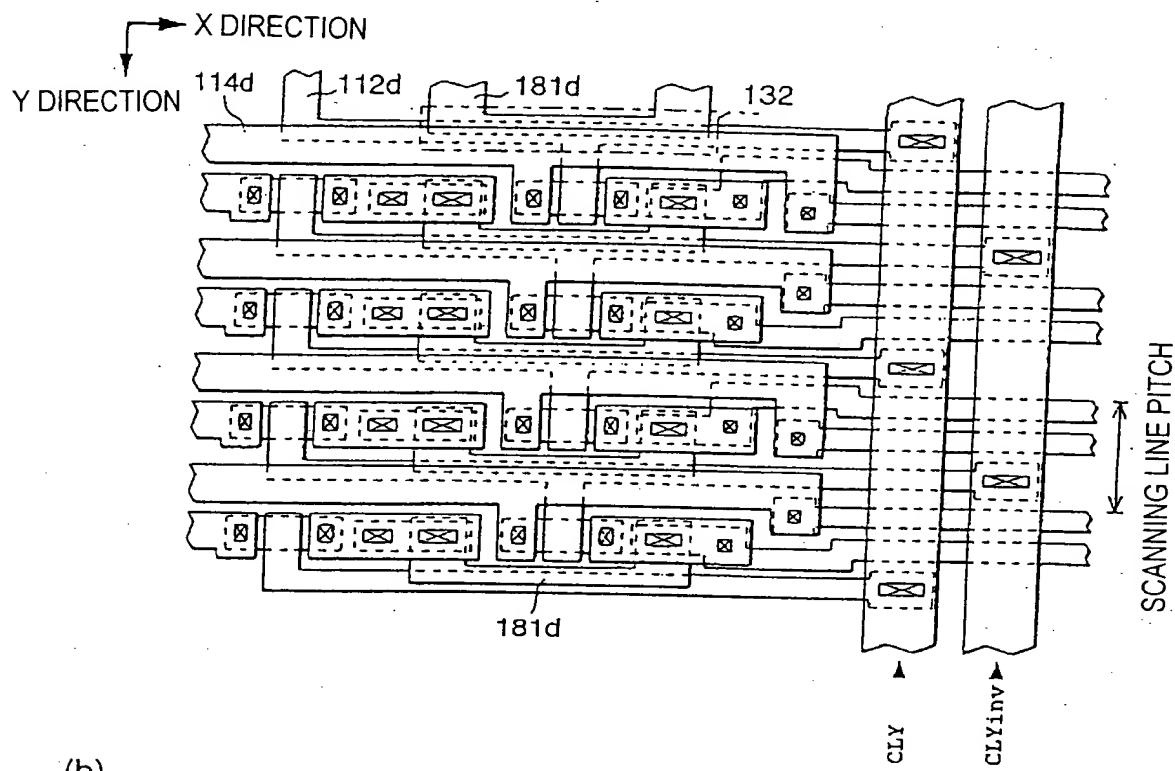


FIG. 9

(a)



(b)

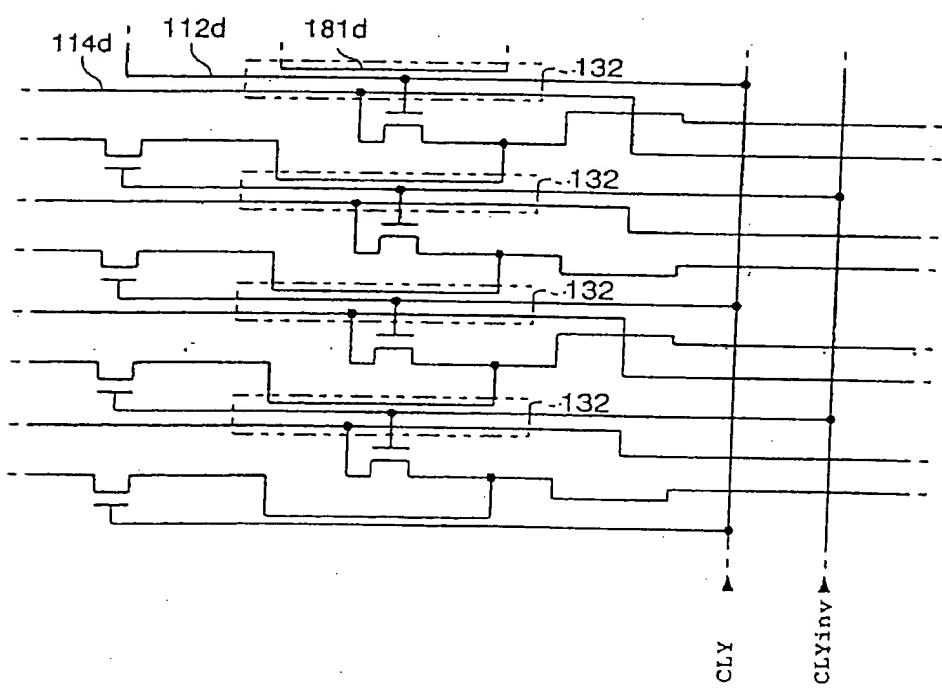
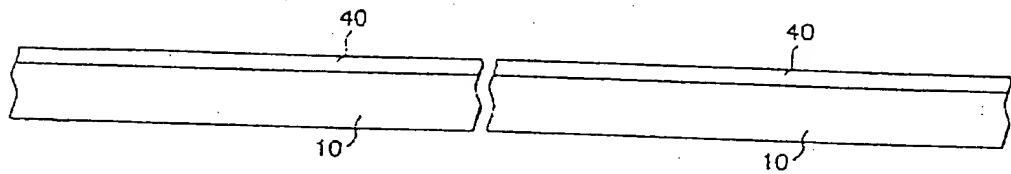


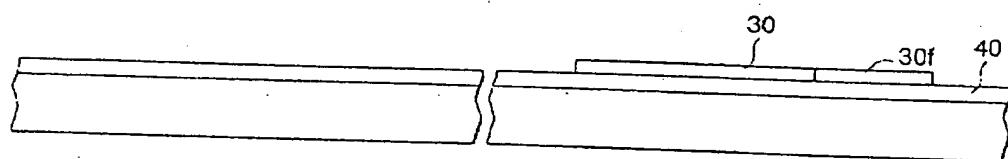
FIG. 10 |

(1)

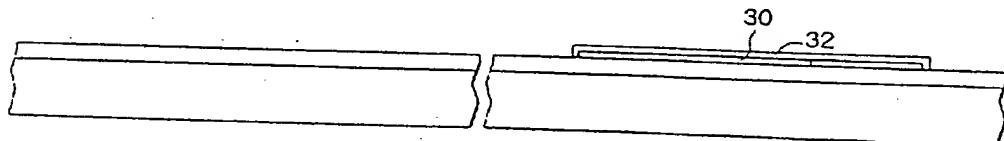
PERIPHERAL CIRCUIT REGION DISPLAY REGION



(2)



(3)

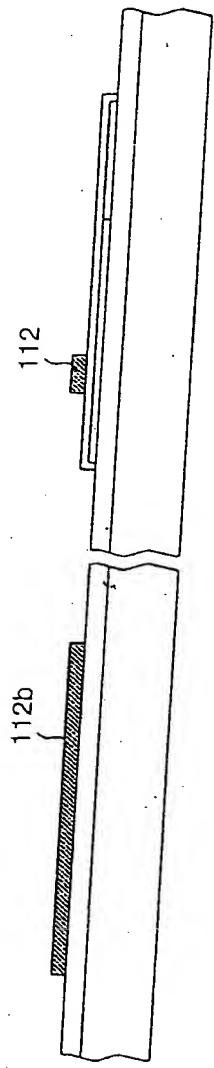


TOP SECRET//NOFORN

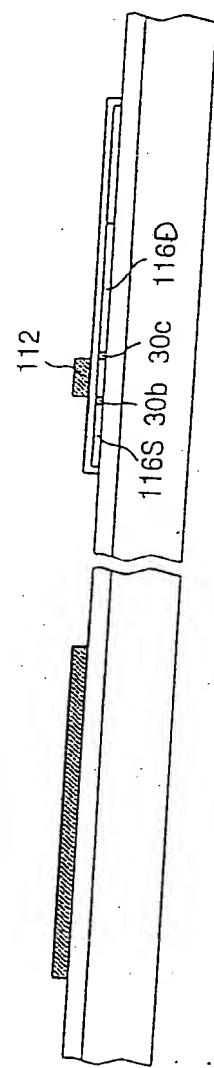
FIG. 11

FIGURE 11 "DRAFTS OF FIG. 10

(4)



(5)



(6)

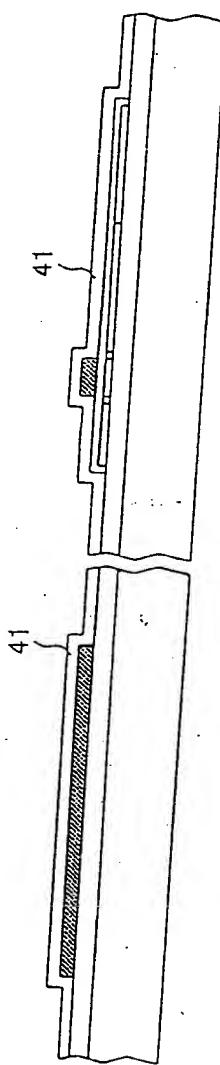
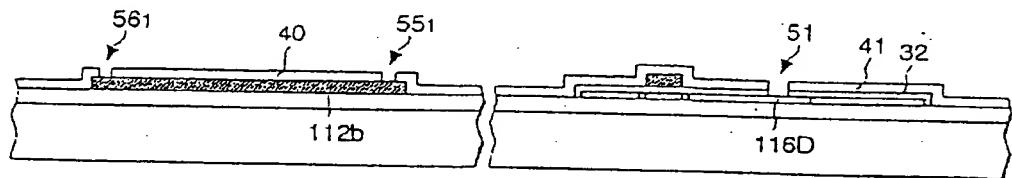
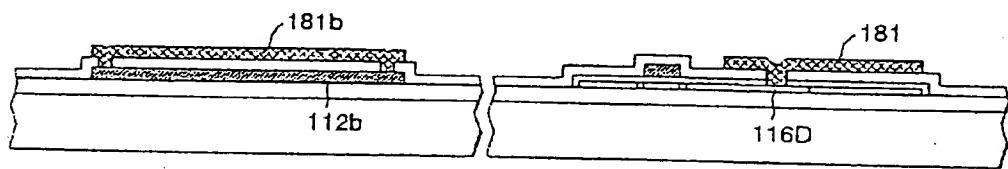


FIG. 12

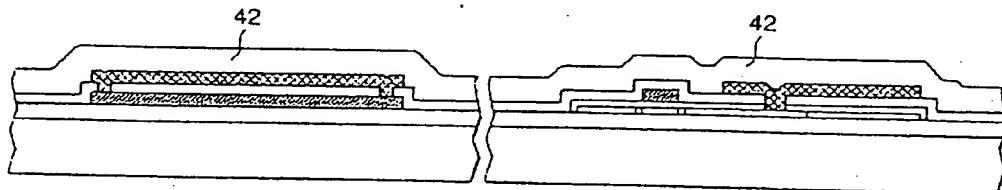
(7)



(8)



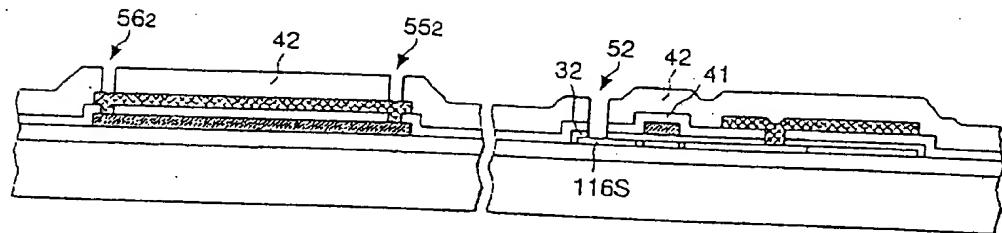
(9)



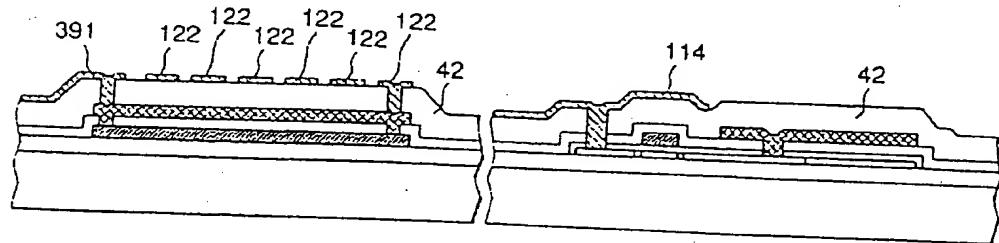
1024150 02499260

FIG. 13

(10)



(11)



(12)

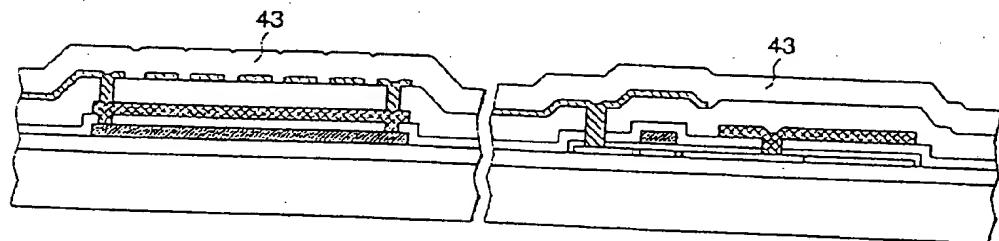
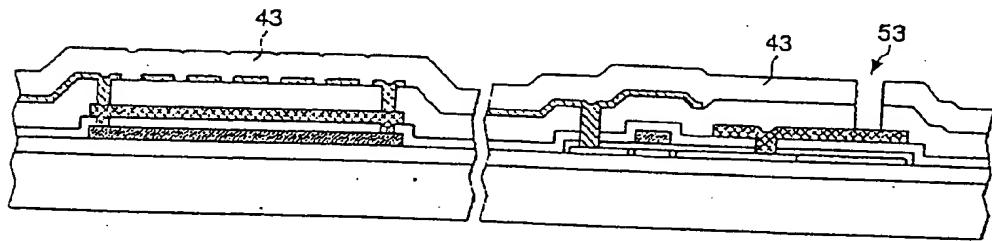
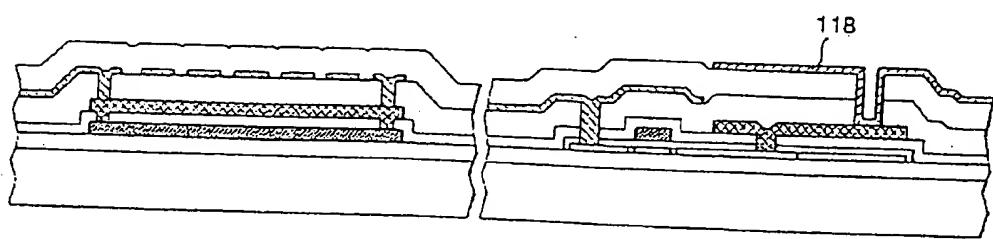


FIG. 14

(13)



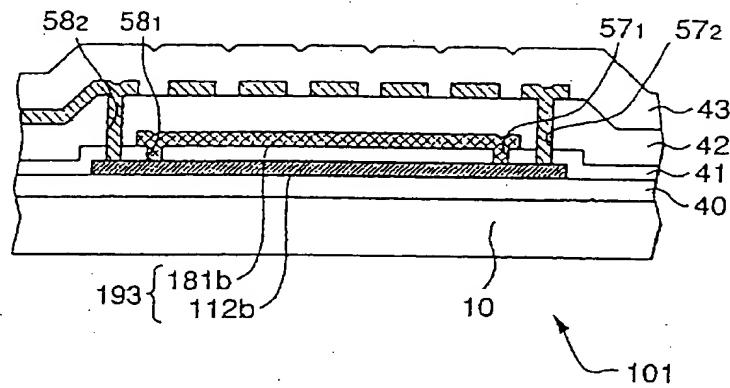
(14)



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FIG. 15

(a)



(b)

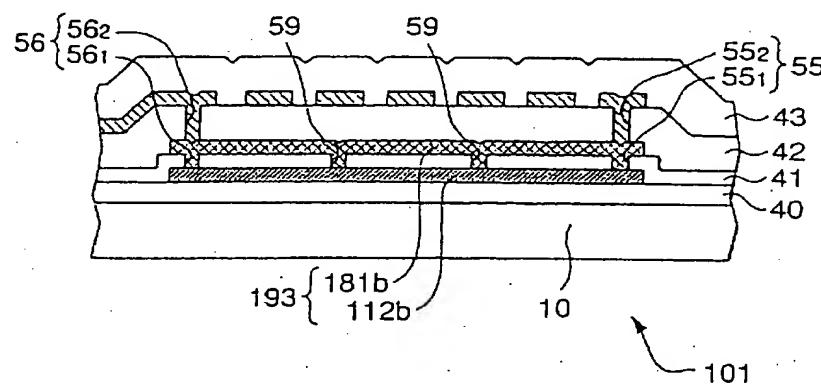


FIG. 16

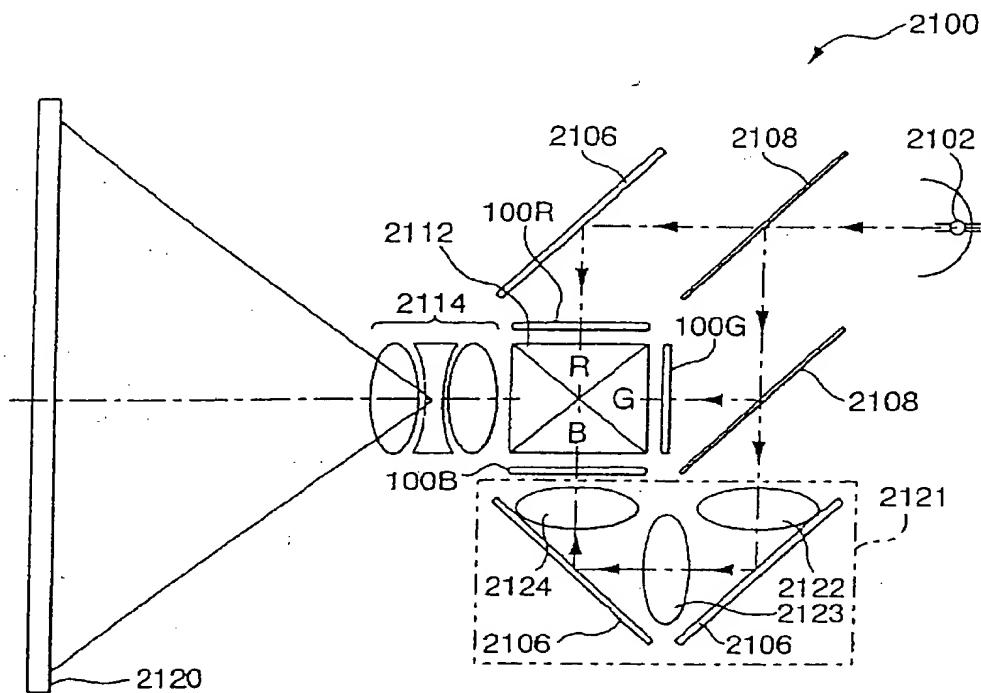


FIG. 17

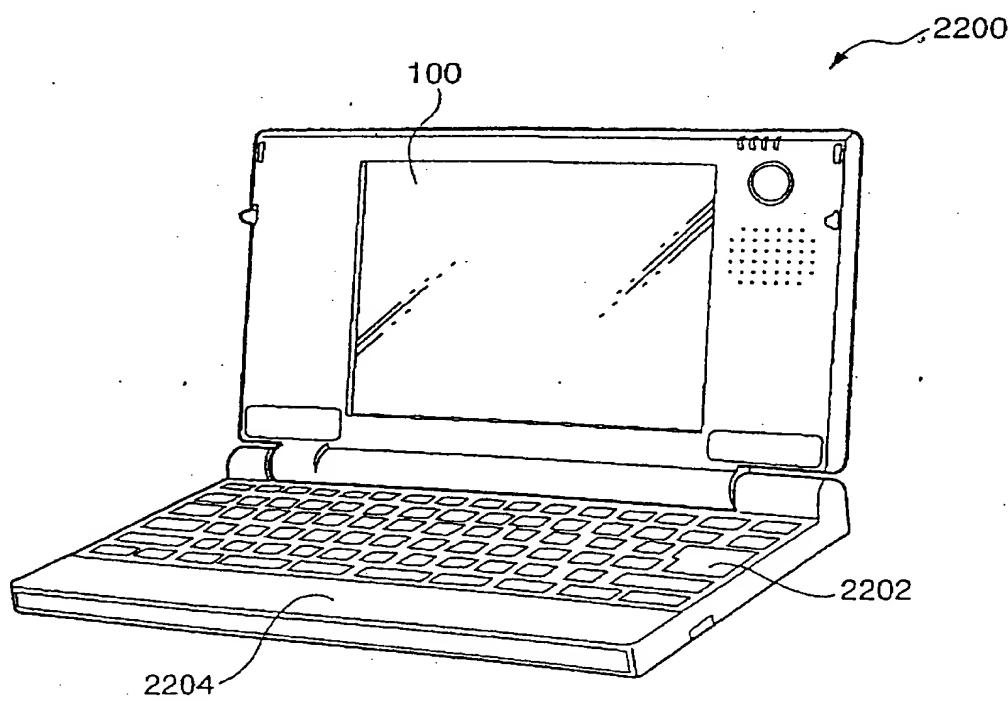


FIG. 18

